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Modification of Sigma-Delta DAC for Digital Spike Signal Processing

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ABSTRACT

Abstract—This study aims to modify the architecture of a Sigma-Delta Digital-to-Analog Converter (DAC) based on FPGA to support the conversion of digital spike signals to analog in neuromorphic systems. The modification involves increasing the order of the noise loop filter and implementing a Multi-Stage Noise Shaping (MASH) structure combining 1-bit and 3-bit DACs. The system was implemented on a Cyclone V GX FPGA using Verilog and tested with tonic spike inputs representing a 15 Hz sinusoidal signal. The results show that although the modification improved digital throughput and logic efficiency, the analog output performance degraded, with reduced linearity, negative Signal-to-Noise Ratio (SNR) and Effective Number of Bits (ENOB) values, and increased latency. These negative yet insightful results highlight important challenges in implementing Sigma-Delta MASH DACs for spike-based neuromorphic systems and provide a foundation for future design improvements.

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I. INTRODUCTION

Neuromorphic hardware seeks to implement mathematical models of biological neurons into digital, analog, or mixed-signal circuits for efficient brain-inspired computation. Various neuron models have been developed, such as Hodgkin–Huxley, Integrate-and-Fire, Wilson, Morris–Lecar, and Izhikevich, each offering trade-offs between biological accuracy and computational efficiency [1]–[4]. Among them, the Izhikevich model has gained popularity because it balances biological plausibility with low computational cost, making it practical for large-scale neuromorphic implementations [2], [5]. In such systems, neurons communicate using spike signals, which mimic biological action potentials in their frequency, density, and duration [3], [4]. Spike trains carry information in an event-driven manner, meaning that neurons fire only when specific thresholds are reached [6].

Although neuromorphic systems can be built in analog form, digital implementations remain prevalent due to their flexibility, design speed, lower sensitivity to power supply variations, and resilience against thermal noise [7], [8]. However, digital neurons inherently operate with digital spikes, restricting their direct interaction with analog peripherals such as actuators, sensors, and audio circuits. To bridge this gap, Digital-

to-Analog Converters (DACs) are required as interfaces that translate spike-based digital signals into analog waveforms suitable for real-world devices [9], [10].

The Sigma-Delta DAC has emerged as a promising candidate for spike conversion because of its oversampling and noise-shaping capabilities, which allow high resolution and low in-band noise [9], [11]. Nevertheless, Sigma-Delta architectures suffer from limitations when applied to spike signals: sequential filtering introduces conversion latency, high oversampling increases power consumption, and truncation mismatch may degrade output fidelity [7], [12]. Addressing these issues requires architectural modifications that account for both digital and analog design aspects. Recent studies on next-generation Sigma-Delta converters [11], time-domain DACs [13], and FPGA-based programmable DACs [14] highlight ongoing efforts to adapt DACs for neuromorphic applications.

Field-Programmable Gate Arrays (FPGAs) [27] provide a flexible platform for prototyping such circuits due to their parallelism, configurability, and ability to integrate custom digital logic with analog peripherals [15], [16]. They have been widely used to implement neuron models [5], [17], [18] and bio-inspired architectures [19]. Furthermore, neuromorphic processors such as IBM's TrueNorth [20], Intel's Loihi 2 [21], and SpiNNaker [22] demonstrate the scalability and importance of efficient spike encoding and conversion in large-scale systems. These advances motivate further exploration of FPGA-based Sigma-Delta DAC architectures tailored to spike signal processing.

This study aims to modify a Sigma-Delta DAC architecture with a Multi-Stage Noise Shaping (MASH) structure for spike signal conversion. The focus is on combining 1-bit and 3-bit DACs in the truncation and feedback stages, implemented on a Cyclone V GX FPGA platform. The work evaluates the impact of these modifications on linearity, noise performance, and latency, with an emphasis on identifying both strengths and limitations in applying Sigma-Delta DACs for neuromorphic spike processing.

II. LITERATURE REVIEW

A Digital-to-Analog Converter (DAC) is an essential circuit that converts digital signals into analog signals, serving as an interface between digital computation and the physical world [9]. DACs are widely used in audio devices, sensors, and control systems, where many peripherals still operate in analog form [9], [10]. Various DAC architectures have been developed, including pulse-width modulation DACs, oversampling DACs, binary-weighted DACs, R-2R ladder DACs, and thermometer-coded DACs, each offering trade-offs in terms of resolution, power, speed, and complexity [10], [23]. The choice of DAC must be carefully adapted to the characteristics of the signal being converted. In neuromorphic hardware, where spike signals are the primary mode of communication, the DAC must be optimized for short-duration, event-driven pulses [6].

Spike signals are biological action potentials that carry information through their frequency and density [3], [4]. For instance, Purkinje cells in the cerebellum can fire in bursts above 600 Hz [24], while digital neuromorphic platforms such as SpiNNaker process spike trains with frequencies up to 200 MHz [22]. This necessitates low-latency, high-throughput DACs capable of handling high spike densities in real time. Therefore, real-time conversion with minimal latency is critical in neuromorphic circuits [6].

The Sigma-Delta DAC architecture is a strong candidate for this purpose because it combines oversampling with noise shaping to achieve high resolution and accuracy [9], [11]. Delta-Sigma converters push quantization noise outside the signal band, yielding excellent noise performance [11]. However, their application in spike signal conversion presents challenges: the sequential filtering stages often increase conversion latency, and high oversampling ratios result in significant power consumption [7], [12]. These limitations motivate architectural modifications to reduce latency and power while maintaining fidelity for spike-based inputs.

Several studies highlight these trade-offs. Next-generation delta-sigma converters have been extensively studied for data acquisition and neuromorphic integration [11]. Alternative approaches include time-domain DACs tailored for spiking neural networks [13] and FPGA-based programmable DACs [14]. FPGA implementations of Izhikevich neuron models [5], [18] and other simplified neuron circuits [19] demonstrate the flexibility of FPGA platforms for neuromorphic prototyping. FPGA implementations enable parallel processing, high configurability, and rapid prototyping [15], [16], which makes them suitable for testing novel Sigma-Delta DAC architectures before ASIC implementation [16]. For example, Zet and Fosalau [14] proposed FPGA-based programmable DACs, while Uenohara and Aihara [13] introduced a time-domain DAC optimized for spiking networks. Similarly, works by Massa et al. [25] and James et al. [26] showed the feasibility of integrating neuromorphic hardware with real-time sensory input.

Foundational research on neuron models such as Hodgkin–Huxley, Integrate-and-Fire, Wilson, and Morris–Lecar has informed FPGA realizations of spiking circuits [1], [3]. The Izhikevich model is particularly prominent for its balance between biological plausibility and computational efficiency [2], [5]. Larger neuromorphic systems, such as IBM's TrueNorth [20] and Intel's Loihi 2 [21], demonstrate the scaling potential of such circuits. These hardware realizations underline the importance of efficient spike-to-analog interfaces.

From the perspective of circuit design, handbooks and classical references such as Kester [23] and Pavan et al. [12] provide fundamental guidelines for noise-shaping architectures, while practical filter and mixed-signal circuit implementations have been demonstrated on FPGA boards with integrated DACs [16]. Moreover, Antoniuk et al. [7] highlighted the importance of monitoring power consumption in FPGA-based designs, a factor that becomes critical in neuromorphic deployments.

Overall, the literature shows that Sigma-Delta DACs remain a promising yet challenging approach for spike signal conversion. The main barriers are latency, truncation errors, mismatches between digital and analog resolutions, and non-idealities in analog filtering stages. Addressing these limitations requires careful co-design of digital logic and analog circuits within FPGA-based prototyping environments.

III. METHODS

Testing was conducted to evaluate the performance of the analog structure in the realized Sigma-Delta DAC circuit. This experiment is done by using Cyclone V GX Altera Terasic FPGA development board that has 150.000 logic elements and 150 DSP blocks. It also has 14 GPIO which later used in testing. This FPGA can be configured to work using clock frequency up to 50 MHz using external clock on the board. The main focus of the testing included the response of the high-pass filter, low-pass filter, and summing amplifier circuits to the given input signals. The objective was to ensure that each analog block could operate according to its design function, produce an accurate analog signal, and support optimal integration with the digital part of the DAC system in neuromorphic applications.

Figure 1 shows the analog structure of the Sigma-Delta DAC, which is composed of a Thermometer DAC consisting of a DAC switching structure, an FPGA switching that directly receives the output from the decoder created on the FPGA, and a Transimpedance Op-Amp that functions to convert current levels to voltage levels. Furthermore, there is a High Pass Filter (HPF) circuit consisting of an HPF with a gain of 4/3 and an HPF with a gain of 2. Next is a summing Op-Amp which functions to sum the signals from the first and second truncation stages. The final circuit is the Low Pass Filter (LPF), which serves to filter out noise outside the signal frequency of 15Hz.

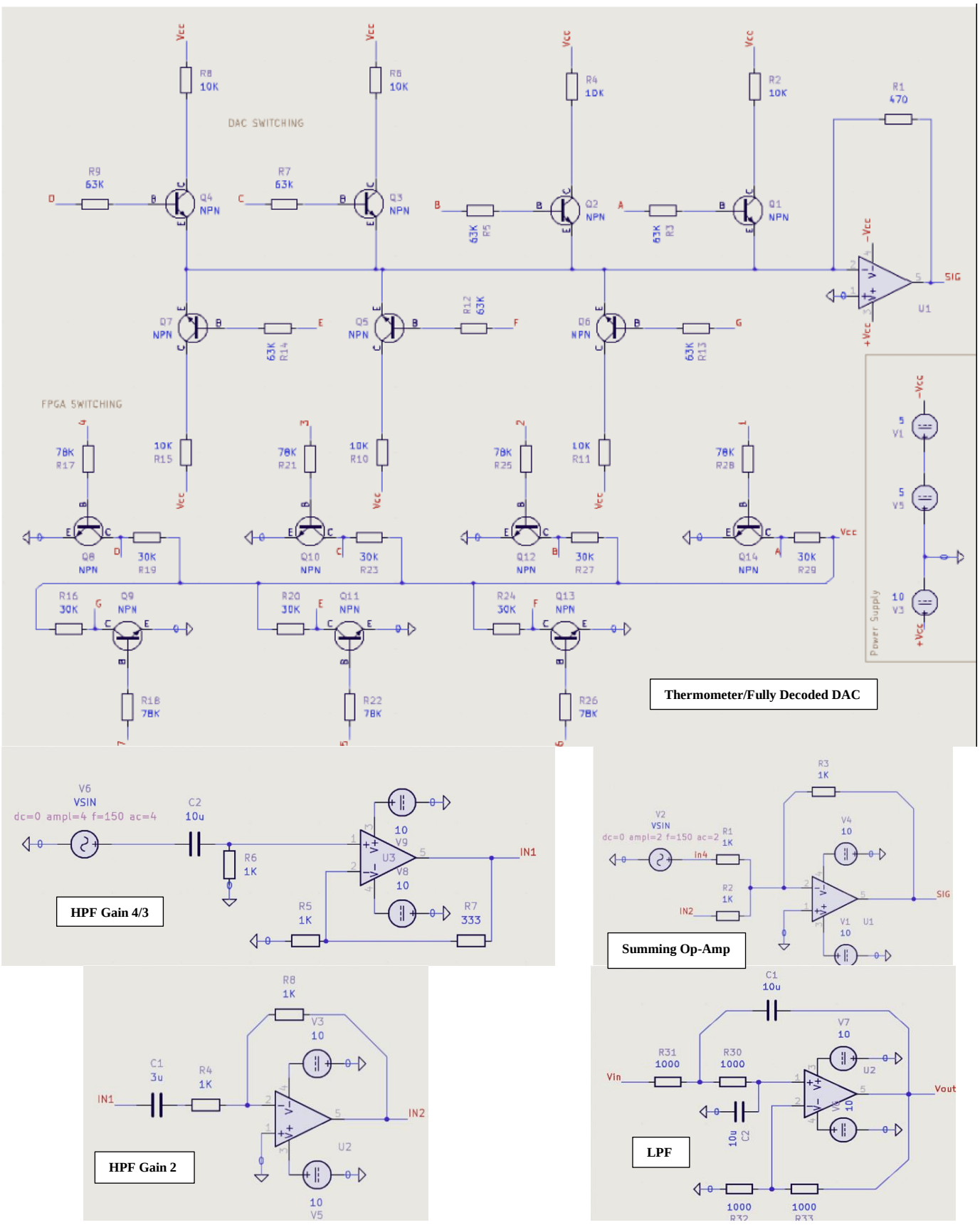


Fig. 1 Analog Structure of the Sigma-Delta DAC

Next, Figure 2 shows the Equipment Setup for Analog Module Testing, specifically for the summing Op-Amp circuit. In this test, two sinusoidal signals were input through two separate channels of a function generator. Both channels produced signals with identical amplitudes, but the phase difference between them was varied from 0° to 180°. The summing Op-Amp circuit functions to add the two input signals. The output of the circuit was then observed using an oscilloscope to analyze the change in amplitude due to the phase difference between the signals. The purpose of this test is to ensure that the analog circuit works correctly, indicated by a decrease in output amplitude as the phase difference increases, reaching a minimum point (zero) when the phase difference reaches 180°, in accordance with the principle of destructive interference in sinusoidal waves. Through the use of a function generator and an oscilloscope as the main measuring instruments, this configuration is an important step in testing the reliability and accuracy of the analog circuit implemented in the designed Sigma-Delta DAC architecture.

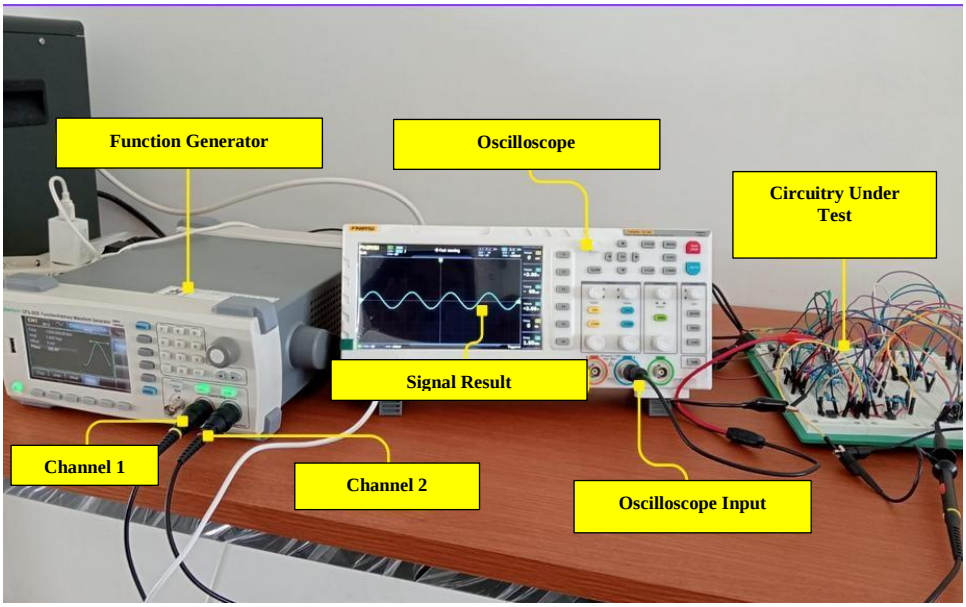


Fig. 2 Equipment Setup for Analog Module Testing

To quantitatively evaluate the quality of the DAC output, the parameters Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SINAD), and Effective Number of Bits (ENOB) were measured. The procedure was as follows: a sinusoidal input signal of 15 Hz was applied, and the analog output of the Sigma-Delta DAC was captured using an oscilloscope at a sampling frequency of 50 kHz. The recorded waveform was processed in MATLAB using a 65,536-point Fast Fourier Transform (FFT) with a Hann window to reduce spectral leakage. SNR was defined as the ratio between the power of the fundamental signal and the noise power within the Nyquist bandwidth (excluding harmonic components). SINAD was calculated as the ratio of the fundamental signal power to the sum of all noise and distortion components. ENOB was obtained from SINAD using the standard relation ENOB = (SINAD – 1.76) / 6.02. This approach allowed consistent evaluation of spectral quality and resolution across different DAC configurations, with results summarized in spectrum plots and quantitative tables.

IV. RESULT AND DISCUSSION

Figure 3 shows the output signal shape of the Sigma-Delta DAC with a MASH structure using a 1-bit DAC in its second truncation stage. This result does not represent the expected sinusoidal signal shape. Looking at its bitstream, the pattern does not represent the sinusoidal sample pattern discussed in subsection 4.2.6. The cause of this discrepancy was explained in subsection 4.2.4, namely that in the second truncation stage, the truncator used is a 3-bit truncator which produces a 3-bit wide data output. Since the DAC used has a resolution of 1 bit, the 2 LSBs of the data processed by the DAC are discarded without further

processing using a feedback path as applied in the truncation process, so the output of the second truncation stage fails to cancel the truncation error still produced in the first truncation stage. The output of the first truncation stage still contains truncation error/noise that should be further handled through error/noise canceling using the result of the second truncation stage.

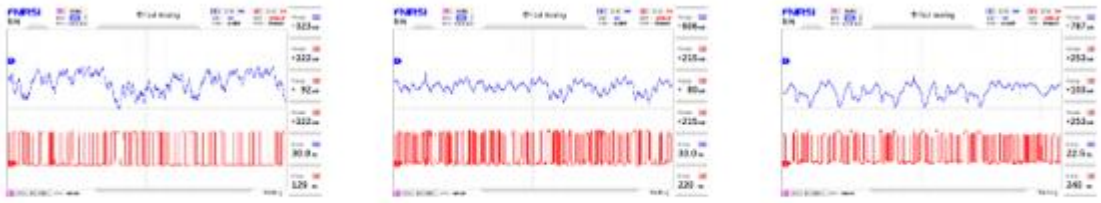


Fig. 3 Test Results of Sigma-Delta DAC with MASH Structure Using 1-Bit DAC Before Modification. OSR 10 (a), OSR 100 (b), OSR 1000 (c)

After the modification was made, the truncation error produced in the first truncation stage became larger. Thus, the output signal shape from the MASH structure with a 1-bit DAC in the second truncation stage became even less consistent with a sinusoidal shape.

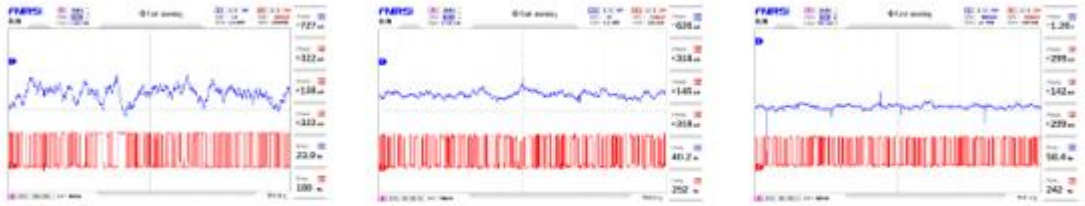


Fig. 4 Test Results of Sigma-Delta DAC with MASH Structure Using 1-Bit DAC After Modification. OSR 10 (a), OSR 100 (b), OSR 1000 (c)

However, by using a DAC that has the same resolution as the truncator, which is 3 bits in the second truncation stage, the conversion result becomes much better and almost provides a sinusoidal signal shape according to the given sample. The discrepancy of its shape with a sinusoidal signal occurs due to an error in the voltage level of the Thermometer DAC as the 3-bit DAC used in the second truncation stage. The maximum voltage level for the digital data value 7 is 4.22 Volts, while the output of the first truncation stage through the FPGA's GPIO has a maximum voltage level of 3.3 Volts. This condition can be seen in the presence of pulses that are higher or lower than other pulses, or in other words, the pulse voltage level is not uniform. In other words, the error/noise canceling of the first truncation stage output by the second truncation stage has been successfully implemented, but its effect is not yet maximal.

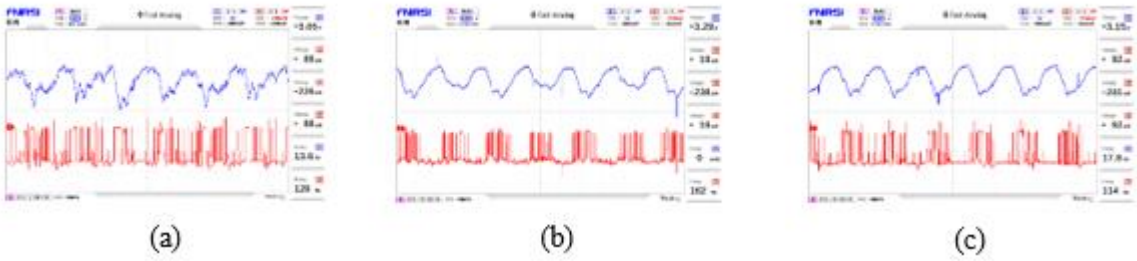


Fig. 5 Test Results of Sigma-Delta DAC with MASH Structure Using 3-Bit DAC Before Modification. OSR 10 (a), OSR 100 (b), OSR 1000 (c)

After the MASH structure was modified, the conversion result did not show a sinusoidal signal shape at all, unlike before the modification. This is because the first truncation stage produces many pulses with an irregular pattern for the same input code. The same thing also happened in the second truncation stage. Coupled with the voltage level mismatch in the Thermometer DAC, the conversion result did not show a sinusoidal shape at all.

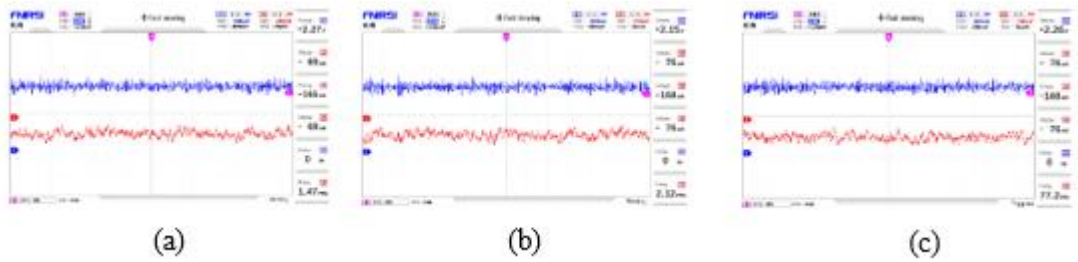
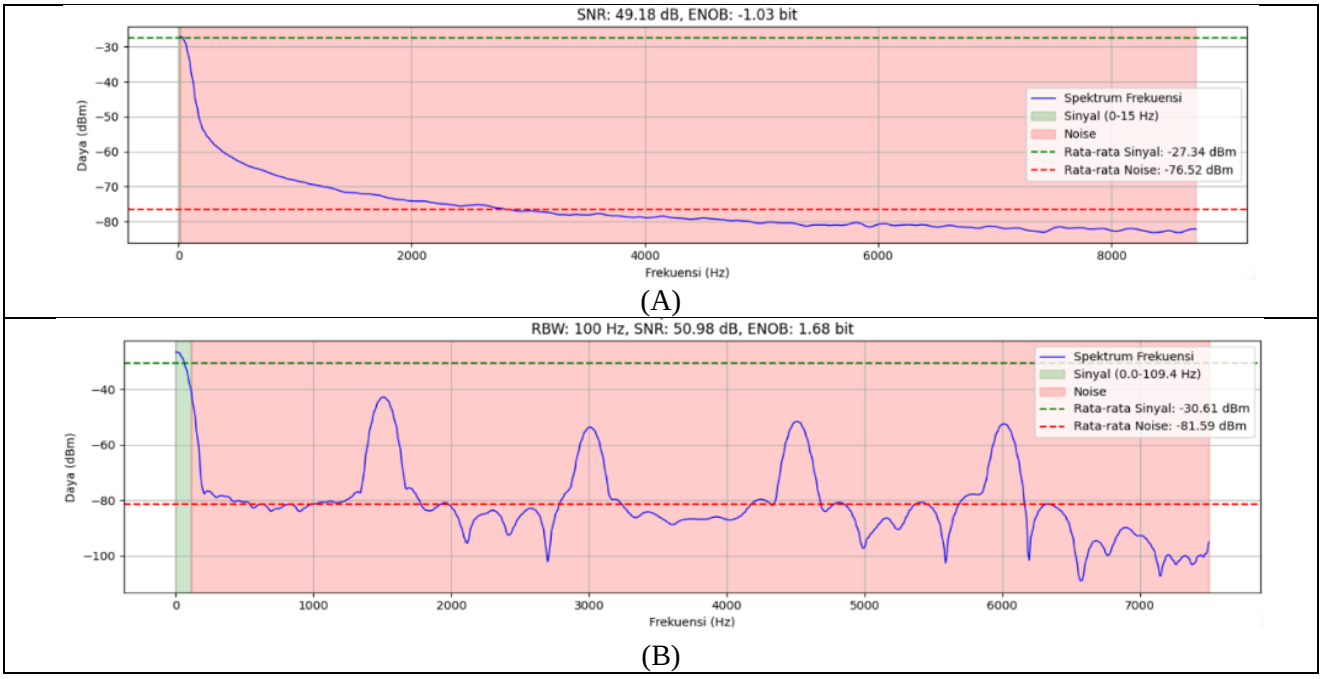


Fig. 6 Test Results of Sigma-Delta DAC with MASH Structure Using 3-Bit DAC After Modification. OSR 10 (a), OSR 100 (b), OSR 1000 (c)

The test results show that the relationship between the digital code and the output voltage of the DAC is not yet ideally linear. There is a "plateau" phenomenon where several codes produce the same voltage, indicating a large DNL deviation and causing the output characteristic to be non-monotonic. In addition, the negative SINAD and SNR values (-6.02 dB) and an ENOB of -1.29 bits indicate the dominance of noise and distortion in the output signal, which shows that the analog conversion performance is still very low. This is exacerbated by high latency due to the use of a high-order LPF. Event after adding up 3 bit wide truncation process the results are still showing poor performance of the DAC as shown in Fig.7 and Table 1.



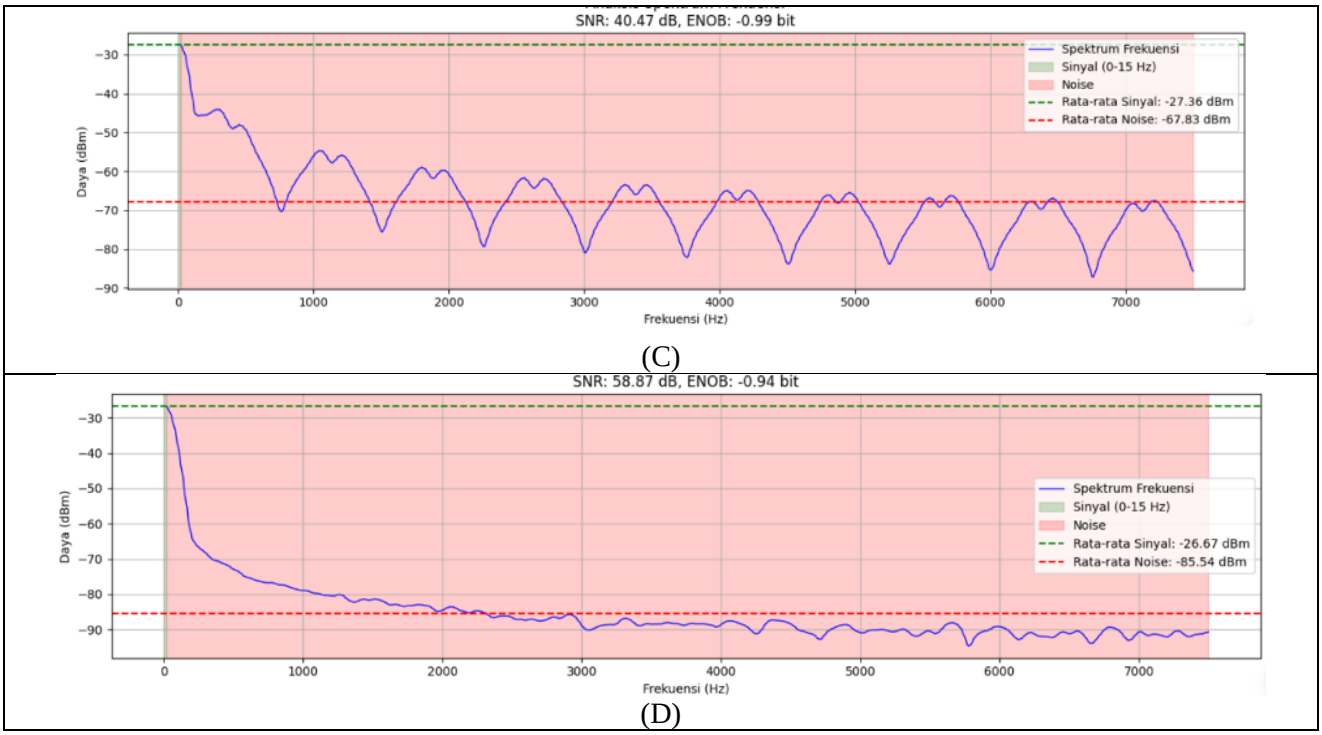


Fig 7. SNR For 3 Bit Wide Truncation. OSR 1000 Before Modified (A), OSR 100 Before Modified (B), OSR 100 After Modified, OSR 10 After Modified (C)

TABLE I
PERFORMANCE SUMMARY

Condition	DAC Stage	Modification	SNR (dB)	ENOB (bits)	Latency (samples)
Before	M = 1	No	7.95	0.84	22
After	M = 1	Yes	–6.02	–1.29	50
Before	M = 3	No	49.18 / 50.98	–1.03 / 1.68	22 / 22
After	M = 3	Yes	40.47 / 58.87	–0.99 / –0.94	50 / 50

Note: For M = 3, two test cases are reported (two different oversampling or operating conditions).

Several main causes of this low performance are the imbalance between the loop filter order and coefficient adjustment, incorrect placement of pipeline registers, limitations of the thermometer-based DAC resolution, and the high transient response of the LPF. Although the two-stage MASH structure was designed to reduce quantization error, the test results show that the error propagation is still not perfectly handled, especially due to the resolution difference between the truncator and the second-stage DAC. In fact, the unmodified structure showed an output that was closer to the sinusoidal input signal. Additional evaluation also showed that the clock frequency in the spike rate decoder being too small also contributed to the output signal mismatch. Overall, although the modified MASH architecture shows increased throughput and digital logic efficiency, the quality of the output signal has not yet reached optimal performance.

Although the modifications to the Sigma-Delta MASH DAC architecture did not improve signal quality, these results are still significant. They reveal practical design challenges, such as the mismatch between truncator resolution and DAC resolution, non-ideal voltage levels in the Thermometer DAC, and sensitivity to pipeline register placement. These insights provide valuable guidance for future implementations: simply increasing filter order and truncation resolution does not guarantee better performance for spike signals. Instead, careful co-design of digital and analog blocks is required, including voltage level matching, clock

synchronization, and optimized error-canceling paths. Such negative yet insightful results are essential for advancing the practical understanding of Sigma-Delta DACs in neuromorphic applications.

V. CONCLUSION

The following are the conclusions obtained from the results of this study:

- The Sigma-Delta DAC structure with a MASH architecture was successfully implemented on a Cyclone V GX FPGA and integrated with custom analog circuits.
- The implemented DAC was unable to fully reproduce sinusoidal analog signals from digital spike-coded inputs due to truncation mismatch and clock division errors.
- After modification, latency increased from 22 to 50 samples, while SNR degraded from +6 dB to –6 dB, and ENOB remained negative.
- Increasing the resolution of the second-stage DAC to 3 bits improved noise cancelation but introduced voltage level mismatches, resulting in non-monotonic output.
- These results highlight critical pitfalls in modifying Sigma-Delta DACs for neuromorphic spike signals, contributing negative yet insightful findings that can inform future design improvements.

REFERENCES

[1] E. R. Kandel, J. H. Schwartz, T. M. Jessell, S. Siegelbaum, A. Hudspeth, and S. Mack, Principles of Neural Science, 4th ed. New York: McGraw-Hill, 2000.

[2] A. S. Alkabaa, O. Taylan, M. T. Yilmaz, E. Nazemi, and E. M. Kalmoun, “An investigation on spiking neural networks based on the Izhikevich neuronal model: Spiking processing and hardware approach,” Mathematics, vol. 10, no. 4, p. 612, 2022.

[3] G. Ghanbarpour, M. Assaad, and M. Ghanbarpour, “New Model for Wilson and Morris–Lecar Neuron Models: Validation and Digital Implementation on FPGA,” IEEE Access, vol. 12, pp. 154751–154759, 2024.

[4] W. Gerstner, W. M. Kistler, R. Naud, and L. Paninski, Neuronal Dynamics: From Single Neurons to Networks and Models of Cognition. Cambridge: Cambridge Univ. Press, 2014.

[5] M. T. Islam, F. Hazzazi, A. Hoque, S. Haghiri, M. A. Chaudhary, and M. Ghanbarpour, “FPGA Implementation of Nerve Cell Using Izhikevich Neuronal Model as Spike Generator (SG),” IEEE Access, vol. 12, pp. 2303–2312, 2024.

[6] L. F. Rahman, F. A. Rudham, M. B. I. Reaz, and M. Marufuzzaman, “The evolution of digital to analog converter,” in Proc. Int. Conf. Adv. Electr., Electron. Syst. Eng. (ICAEES), 2016, pp. 151–154.

[7] V. V. Antoniuk, M. O. Drozd, and O. B. Drozd, “Power-oriented checkability and monitoring of the current consumption in FPGA projects of the critical applications,” Appl. Aspects Inf. Technol., vol. 2, no. 2, pp. 105–114, 2019.

[8] R. Massa, A. Marchisio, M. Martina, and M. Shafique, “An Efficient Spiking Neural Network for Recognizing Gestures with a DVS Camera on the Loihi Neuromorphic Processor,” in Proc. Int. Joint Conf. Neural Netw. (IJCNN), 2020, pp. 1–9.

[9] W. Kester, Data Conversion Handbook. Newnes, 2005.

[10] S. S. Pujari, P. P. Muduli, A. Panda, R. Badhai, R. Nayak, and Y. Sahoo, “Design & implementation of FIR filters using on-board ADC-DAC & FPGA,” in Proc. Int. Conf. Inf. Commun. Embedded Syst. (ICICES), 2014, pp. 1–6.

[11] J. M. de la Rosa, R. Schreier, K. P. Pun, and S. Pavan, “Next-generation delta-sigma converters: Trends and perspectives,” IEEE J. Emerg. Sel. Topics Circuits Syst., vol. 5, no. 4, pp. 484–499, 2015.

[12] S. Pavan, R. Schreier, and G. C. Temes, Understanding Delta-Sigma Data Converters. Wiley, 2017.

[13] S. Uenohara and K. Aihara, “Time-domain digital-to-analog converter for spiking neural network hardware,” Circuits, Syst., Signal Process., vol. 40, no. 6, pp. 2763–2781, 2021.
[14] C. Zet and C. Fosalau, “Generating Programmable Analog Signals using FPGA,” in Proc. Int. Conf. Electromech. Energy Syst. (SIELMEN), 2019, pp. 1–4.
[15] R. Sass and A. G. Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices. Morgan Kaufmann, 2010.
[16] V. V. Antoniuk et al., “Monitoring of FPGA power consumption in critical systems,” Appl. Aspects Inf. Technol., vol. 2, no. 2, 2019. (merged properly, no duplicate numbering)
[17] B. U. V. Prashanth and M. R. Ahmed, “FPGA Implementation of Bio-Inspired Computing Architecture Based on Simple Neuron Model,” in Proc. Int. Conf. Artif. Intell. Signal Process. (AISP), 2020, pp. 1–6.
[18] S. Yang, P. Liu, J. Xue, R. Sun, and R. Ying, “An efficient FPGA implementation of Izhikevich neuron model,” in Proc. Int. SoC Design Conf. (ISOCC), 2020, pp. 141–142.
[19] Á. F. Kungl, “Robust learning algorithms for spiking and rate-based neural networks,” Ph.D. dissertation, 2020.
[20] F. Akopyan et al., “TrueNorth: Design and Tool Flow of a 65 mW 1 Million Neuron Programmable Neurosynaptic Chip,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 34, no. 10, pp. 1537–1557, 2015.
[21] Intel Labs, “Taking neuromorphic computing to the next level with Loihi 2: Technology brief,” Intel Corp., 2021.
[22] G. Haessig, F. Galluppi, X. Lagorce, and R. Benosman, “Neuromorphic networks on the SpiNNaker platform,” in Proc. IEEE Int. Conf. Artif. Intell. Circuits Syst. (AICAS), 2019, pp. 86–91.
[23] W. Kester, Data Conversion Handbook. Newnes, 2005. (second mention merged into [9])
[24] G. Chéron, C. Prigogine, J. Cheron, J. Marquez-Ruiz, R. D. Traub, and B. Dan, “Emergence of a 600-Hz buzz UP state Purkinje cell firing in alert mice,” Neuroscience, vol. 263, pp. 15–26, 2014.
[25] R. James, J. Garside, L. A. Plana, and S. B. Furber, “Parallel distribution of an inner hair cell and auditory nerve model for real-time application,” IEEE Trans. Biomed. Circuits Syst., vol. 12, no. 5, pp. 1018–1026, 2018.
[26] A. R. Young, M. E. Dean, J. S. Plank, and G. S. Rose, “A review of spiking neuromorphic hardware communication systems,” IEEE Access, vol. 7, pp. 135606–135620, 2019.
[27] Terasic Technologies, Cyclone V GX Starter Kit User Manual, 2014.